CAD Synthesis of Interstage Networks for Multi-Stage Amplifiers with a Wide Range of Topologies

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Abstract

This paper reviews the techniques and capabilities of CAD Synthesis algorithms which have the capability of designing interstage networks with expanded topology selections. This enables the CAD synthesis of multi-stage amplifiers and increases the opportunity to find an optimum design solution. design problem. Specific ultra-wideband amplifier design examples are given which illustrate the effectiveness of the CAD Synthesis algorithms and design techniques.

A. Introduction

In recent years synthesis methods have been successfully applied to the problem of designing matching networks for wideband microwave amplifiers. Many of the available CAD algorithms, however, do not offer the capability of designing interstage networks nor do they offer the full range of topology selections necessary to provide a wide range of flexibility in finding an optimum design solution to a microwave amplifier design problem. This paper reviews the techniques and capabilities of CAD Synthesis algorithms which have the capability of designing interstage networks where arbitrary impedance levels and parasitic elements are present at both ends of the matching network. Also, The ability to design with topologies of arbitrary order (including odd order) and arbitrary number of low-pass and high-pass elements increases the opportunity to find an optimum solution to a given design solution. Specific design examples are given which demonstrate the effectiveness of the CAD Synthesis algorithms and design techniques.

B. The Power of Designing Interstage Matching Networks

The algorithms described in this paper allow specification of arbitrary impedance levels and inclusion of parasitic elements at both ends of a matching network, thus allowing the design of interstage networks. In addition to the specification of any desired source (impedance and parasitic) and load (impedance and parasitic), the designer specifies a desired bandwidth, ripple, gain slope, response type (equiripple or maximally flat) and topology. The CAD Synthesis algorithms provide the matching networks to the given specifications in an automated and time-effective manner. These algorithms thus enable interstage design and provide the following advantages :

-Multi-stage amplifiers can be designed.

-The complexity of the design is decreased because a single interstage replaces two matching networks : an output matching network and an input matching network. This added complexity decreases circuit size, line lengths, circuit loss and the overall cost of the design.

-Frequency response compensation can be readily designed into interstage networks without generating mismatch problems at the input or output of the amplifier.

The operation of the interstage synthesis algorithms is outlined as follows:

-The synthesis algorithm checks the frequency response specification and assures that the required parasitics on both sides of the network can be included before proceeding to synthesize. If necessary the gain of the response is reduced enough to accommodate the required parasitics.

-The synthesis algorithm considers all possible combination of the reflection coefficient zeros to find solutions to accommodate parasitics on both sides of the network. This increases design alternatives and avoids unnecessary reduction of the gain of the network.

-For bandpass networks , transformations on the network provide the necessary impedance shifting without altering the response.

C. More Flexible Topologies

Most CAD synthesis algorithms employ low-pass or low-to-bandpass transformed topologies. This places the following restrictions on topologies:

N = Order = Even

J = Number of high-pass elements = N/2

The algorithms described in this paper enable more flexible topology parameters as follows:

N = Order = Even -or- Odd

J = Number of high-pass elements = 1,2...N/2...N

This greatly enhanced flexibility in the selection of the topology increases correspondingly the design flexibility and the opportunity to obtain a

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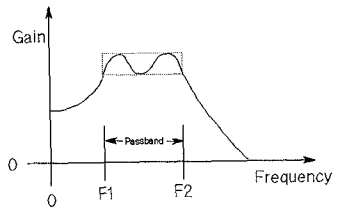
more optimum wideband amplifier design.

For low-pass topologies, a frequency response of the following form is employed in the algorithms:



Since the zero-frequency (dc) response is not part of the passband, the dc response can be specified independently of the passband response. Since the dc response controls the impedance transformation of the network, a desired impedance can be obtained without unnecessary gain reduction in the passband. Note that this approach optimizes the inclusion of parasitic elements while maximizing gain bandwidth, because gain-bandwidth from dc to F1 is not unnecessarily used.

D. Amplifier Design Procedure and CAD Implementation

The design methodology employed is graphically illustrated in Figure 1. As shown in this design methodology, active devices must often be modified with feedback or loading in a wideband amplifier design. to achieve one or more of the following:

-Device stabilization : avoid oscillation

-Frequency response compensation

-Impedance matching : to improve the feasibility of input and output impedance matching over the passband

The design steps outlined in Figure 1 are automated including :

-Device modeling
-Matching network synthesis
-Matching network optimization
-Amplifier compilation from device and matching network files
-Top level amplifier analysis and optimization

Intermediate results are stored as named files for convenient future recall.

E. Design of Two Stage GaAs FET Amplifier with Transmission Line Matching Networks

A two stage amplifier is to be designed to obtain the maximum practical gain over the frequency 4-18 GHz. A distributed realization is desired for implementation purposes. The design process follows the procedure outlined in Figure 1 :

a) The device selected is the NEC 70000 GaAs FET.

b) The feedback and loading scheme is shown in Figure 2. The criterion for this design was to provide frequency response compensation and make the input and output impedances easier to match.

c) The modified device including feedback and loading circuits was then gain and impedance modeled. The resultant device model is shown in Figure 3.

d) The input, output, and interstage matching networks were synthesized to prescribed bandwidth, gain and ripple using the described algorithms. The algorithms assure that needed impedance transformations and parasitic inclusions are made.
The CAD design of the interstage is shown in Figure 4. Note that the topology for this interstage had 8 total elements (before impedance transformation and parasitic extraction) and 5 high-pass elements.

e) The matching networks were individually optimized. At this stage of the design, modeling approximations are removed, and actual device parameters are used.

f) The matching networks were cascaded with the (modified) active devices, then analyzed and optimized.

The resultant Amplifier is shown in Figure 5 and the frequency response in Figure 6. In Figure 6, the gain response is shown before and after top-level optimization. The slight differences in these responses illustrate that the individual matching network designs were very effective.

F. Design of a Two Stage GaAs FET Amplifier with Lumped Matching Networks

A two stage amplifier is to be designed to obtain the maximum practical gain over the frequency 2-18 GHz. The design process follows the procedure outlined in Figure 1 and the preceding design example.

The Completed amplifier is shown in Figure 7 and the resultant response in Figure 8.

G. Design of Two Stage GaAs FET Amplifier with Transmission Line Matching Networks of Low-Pass Form.

A two stage amplifier is to be designed to obtain the maximum practical gain over the frequency 0-18 GHz. The design process follows the procedure outlined in Figure 1 and the preceding design example. Since the design is to operate at dc, the matching structure is chosen to consist of series lines and shunt open stubs : a distributed realization of a low-pass matching structure that will provide dc coupling to the signal.

The Completed amplifier is shown in Figure 9 and the resultant response in Figure 10.

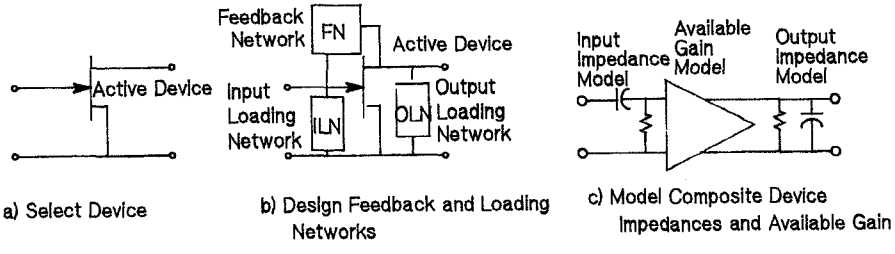
H. Conclusions

CAD Synthesis is a powerful tool for the design of matching networks for wideband microwave amplifiers. This tool is made more powerful and more flexible when the synthesis algorithms are expanded to include interstage design and to allow

more flexible topologies. The amplifier designs illustrated show that very effective designs can be obtained with these enhanced tools, with all of the design steps automated in the CAD Synthesis algorithms.

References

1. W.H. Ku, "Optimum Gain-Bandwidth Limitations of Transistor Amplifiers as Reactively Constrained Active Two-Ports." IEEE Trans. Circuits and Systems, vol. CAS-223, no. 6, pp. 523-533, June 1975.
2. D. J. Mellor and J.G. Linvill, "Synthesis of Interstage Networks of Prescribed Gain versus Frequency Slopes," IEEE Trans. Microwave Theory and Techniques, vol. MTT-23, no. 12, pp. 1013-1020, Dec. 1975.
3. D.J. Mellor, " Improved Computer-Aided Synthesis Tools for the design of Matching Netowrks for Wide-Band Microwave Amplifiers," IEEE Trans. Microwave Theory and Techniques, vol. MTT-34, no. 12 pp. 1276-1281, Dec. 1986.
4. B.S. Yarman and H.J. Carlin, "A Simplified 'Real Frequency' Technique Applied to Broad-Band Multi-stage Microwave Amplifiers, " IEEE Tans. Microwave Theory and Techniques, vol. MTT-30, pp. 2216-2222, Dec. 1982.
5. S.E. Sussman-Fort, "DESIGN: A program for the Automated Synthesis of Broadband Matching Networks Between Complex Terminations," Proceedings RF Expo East, Nov. 10-12, 1986 Boston Mass.
6. M.W. Medly, "Network Synthesis CAD Program Applied to RF and Microwave Circuit Design," Microwave Systems News, January, March and April 1987.



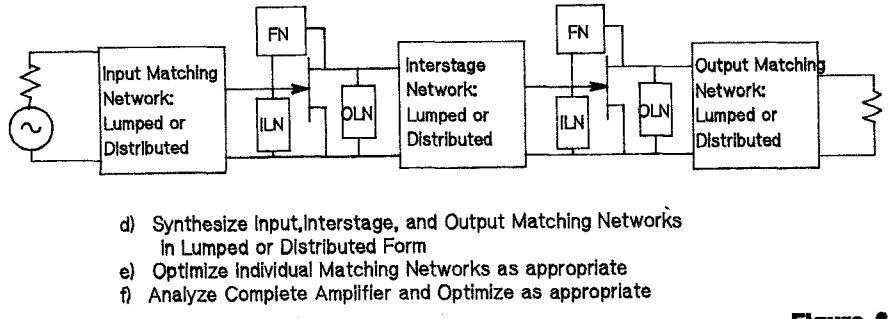


Figure 1. Outline of Amplifier Design Procedure

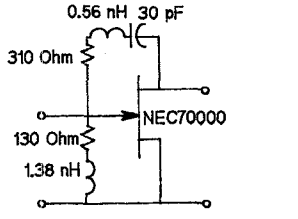


Figure 2. Feedback and Loading Network Design.

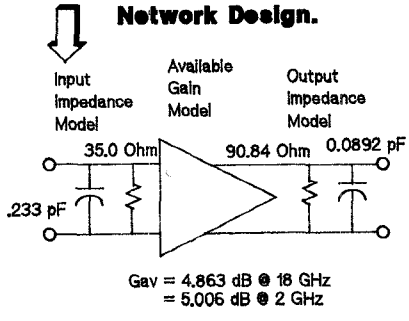


Figure 3. The Impedance and Gain Model of the Composite Device.

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# ELEMENTS =   8.000 # HI PASS =   5.000  SOLUTION  2  /  32   | TEE TRANSFORM
SOURCE RES.=  90.836 DES. LOAD =  35.000 Flower=      4.000 Fupper=     18.000
SLOPE =        0.000 RIPPLE =     0.100 MIN LOSS =   0.100  SHAPE=   ER
ZERO LOCATIONS : COMPLEX ZEROS :  0  0  0  0
 SYNTHESIZED NETWORK      | IMP TRANSFORMED NET |        TRANS LINE NETWORK
*************************************************************************
  SOURCE     90.8363  OHM SOURCE    90.8363  OHM SOURCE    90.8363  OHM
  1 CP        0.102363 pF  CP        0.089006 pF  CP        0.089006 pF
  2 LP        3.301519 nH  CP        0.013357 pF  TLOC      2.163 DEG      25 OHMS
  3 LS        1.336341 nH  LS        0.891917 nH  TLIN     45.249 DEG     100 OHMS
  4 CS        0.246766 pF  LP        2.409602 nH  TLSC     69.850 DEG     100 OHMS
  5 LP        1.640586 nH  LS        0.060874 nH  TLIN      3.938 DEG     100 OHMS
  6 CS        0.426083 pF  CS        0.463257 pF  CS        0.463257 pF
  7 LP        1.224757 nH  LP        0.873900 nH  TLSC     44.665 DEG     100 OHMS
  8 CP        0.269824 pF  CS        0.799891 pF  CS        0.799891 pF
  9LOAD      65.705779 OHM LP        0.652399 nH  TLSC     36.422 DEG     100 OHMS
 10                        CP        0.273178 pF  TLOC     37.682 DEG      25 OHMS
 11                        CP        0.233367 pF  CP        0.233367 pF
 12                      LOAD       34.999884 OHMLOAD      34.999884 OHM
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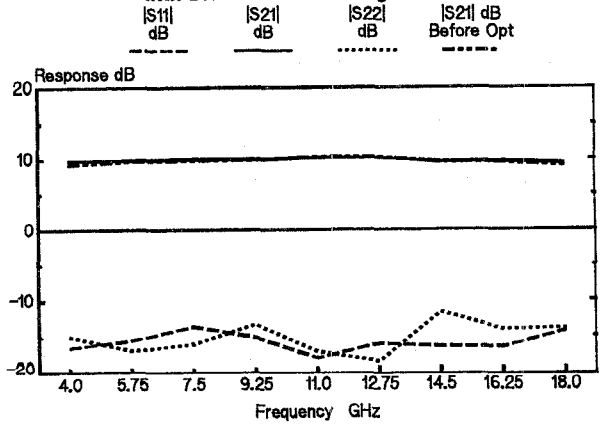
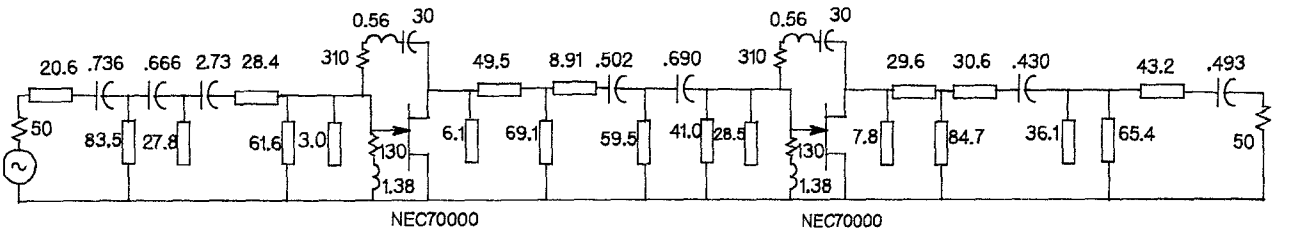
Figure 4. Example Synthesis Design (Interstage for the Amplifier of Figure 5)

Figure 6. Two Stage FET Amplifier with Distributed Matching Networks

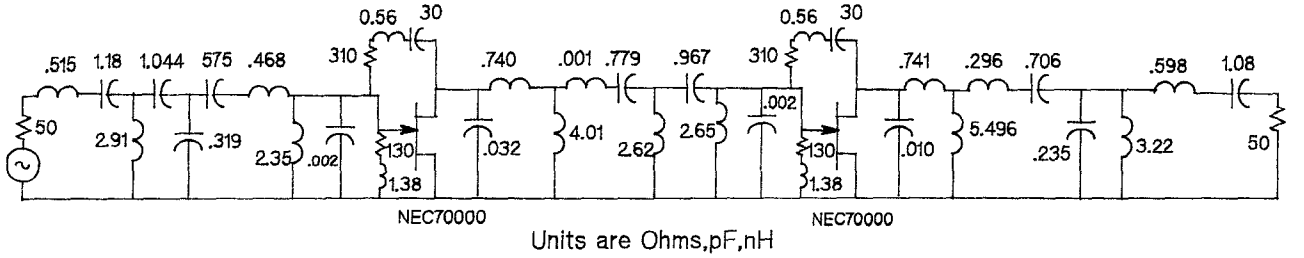




Units are Ohms,pF,nH, and Degrees @ Fu=18 GHZ

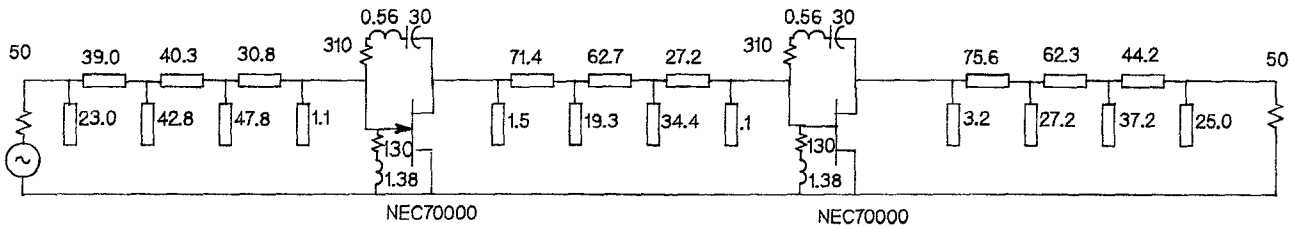
Open stubs are 25 Ohm, Shorted stubs and series lines are 100 Ohm.

Figure 5. Two stage GaAs FET Amplifier with Distributed Matching Networks



Units are Ohms,pF,nH

Figure 7. Two stage GaAs FET Amplifier with Lumped Matching Networks



Units are Ohms,pF,nH and Degrees at fu=18 Ghz.

Series Transmission Lines are 100 Ohm, Shunt Lines are 25 Ohm.

Figure 9. FET Amplifier with Distributed Matching Networks of Low-Pass Form

Figure 8. Two Stage FET Amplifier with Lumped Matching Networks

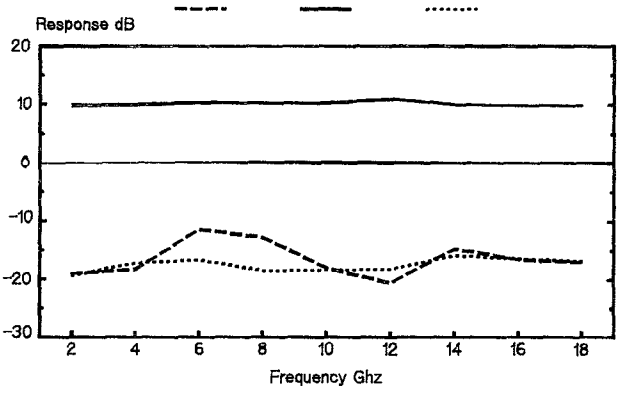


Figure 10. Two Stage FET Amplifier with Distributed Matching Networks of Low-Pass Form